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PowerPC™ Microprocessor Common Hardware Reference Platform: I/O Device Reference

Developed by Apple Computer, Inc., International Business Machines Corporation, and Motorola, Inc.

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About this Document

This document is an extension of the I/O Device chapter in the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture*. The purpose of this document is to define architecture and minimum system requirements for I/O devices. These requirements will govern devices which may be used in CHRP systems. These requirements are intended to be precise enough to assure application software compatibility for several operating system environments, broad enough to cover portables through server platforms in single or multiprocessor configurations, and forward-looking enough to allow evolution, including 64-bit addressing.

These requirements were developed by Apple Computer, Inc., International Business Machines Corporation, and Motorola, Inc. to define a system which is intended to become the pervasive open industry standard for single-user portable through multi-user server configurations. Systems built to these requirements will have PowerPC microprocessor(s) and will share components with the Apple® Macintosh® family and IBM compatible personal computers. These systems will be capable of running various native operating systems. The set of operating systems anticipated to be available includes Apple Mac™ OS, IBM AIX™, and PowerPC™ editions of Microsoft Windows NT™ Workstation and SunSoft Solaris™. Most applications for these operating environments may be run on these systems either in native mode or through some emulation capability. With the appropriate operating system and x86 emulation support, these systems will be capable of running Windows™ and DOS applications.

Within the context of this document, “architecture” is defined as the specification of the interface between the hardware platform and the operating systems and applications. Device drivers also use this architecture, but require additional definition of the operating system interfaces.

To the extent that firmware abstracts the hardware interface, it becomes part of the hardware. The firmware to operating system interface is defined in this architecture. Two types of firmware are discussed here. Open Firmware is the initialization or boot code that controls the platform prior to the transfer of control to the operating system. Run-Time Abstraction Services (RTAS) is the run-time firmware which provides abstractions to the executing operating system. Interfaces within the software or within the hardware are not defined in this document. Where necessary, reference will be made to documents where those definitions can be found.

Within the context of this document the term “the architecture” or “the CHRP architecture” is used to refer to the requirements contained in the document, *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* [1] and this extension, *PowerPC Microprocessor Common Hardware Reference Platform: I/O Device Reference* [11].

Goals of this Specification

The specific goals of this specification are as follows:

- To document the architecture at a register level for native I/O devices. Some devices are documented by manufacturer neutral documents and these documents will be referred to as the source of this architectural definition. Other devices are only defined by current implementations. Where a single commonly used

implementation exists we will document it. When several competing implementations are in current use we will document a subset which provides some component vendor choice.

- To create an open industry standard to be used for the implementation of PowerPC based systems. The architecture document is available to the industry and can be used by any hardware or software vendor to develop compliant products.
- To allow compatible differentiation through the use of abstracted hardware interfaces, defined minimum hardware, and extension mechanisms.
- To leverage existing and future industry-standard buses and interfaces. Existing bus architectures have a proven level of performance and functionality. Established industry-standard interfaces—for example SCSI, IDE, LocalTalk®, Ethernet™, etc.— and newer bus architectures, interfaces and protocols —for example PCI, PC Card, IrDA, etc.— provide higher levels of performance or utility not achievable by the older standards. The architecture allows platform and system designers to determine which buses, interfaces, and protocols best suit their target environment.
- To provide an architecture which can evolve as technology changes. The creators of the architecture invite industry participation in evolving future versions of it.

Audience for this Document

This document defines the architecture and system requirements for I/O devices to be used in building PowerPC platforms which comply with the Common Hardware Reference Platform (CHRP™). This document is the source of information that a hardware platform, operating system, or hardware component developer would need to create compatible products. Additional requirements are defined by the industry standards referenced in this document.

This document must be used by those building CHRP systems. The document describes the hardware to operating system interface which must be provided for I/O devices in these platforms. Platform designers must assemble components and firmware which match this interface. Also, the document defines minimum I/O device configuration requirements. Platform designers must meet or exceed these minimums to build a CHRP system. The operating systems which are expected to support this architecture are listed in an appendix for the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* [1]. Each operating system has configuration requirements which are described in documents maintained by the owners of the operating systems. Using these requirements, a hardware platform designer may target a configuration to support multiple operating systems.

This document must be used by those building compatible software including operating systems, device drivers, boot software, or firmware. If a function is supported, software developers must provide support for the interfaces described in this document. This software must provide the mandatory functions and capabilities as described in the requirements in this document. However, this document does not limit this software from going beyond the specification through software tailored to specific hardware.

Component manufacturers will use this information to produce compatible I/O chips and adaptors to use on these platforms.

Organization of this Document

The following chapters provide the detailed requirements for I/O devices to be used in compliant systems. Where appropriate, references are made to other industry standards or readily available reference documentation for the required architecture information.

Following is a summary and brief description of the chapters and appendices of this document:

- Chapter 1, “General Requirements and Information,” on page 1 gives some requirements which apply to all devices and acknowledges the source of some of this material.
- Chapter 2, “ISA DMA Controller,” on page 3 defines the ISA direct memory access controller requirements and programming model.
- Chapter 3, “Floppy Disk Controller,” on page 31 gives the requirements for the floppy disk controller.
- Chapter 4, “Legacy Interrupt Controller,” on page 61 sets the requirements for the interrupt controllers which are a legacy from IBM compatible PCs.
- Chapter 5, “Parallel Port Controller,” on page 79 defines the requirements for the parallel port.
- Chapter 6, “UART Controller,” on page 93 sets the requirements for the serial communications controller which is a legacy from IBM compatible PCs.
- Chapter 7, “ISA Keyboard/Mouse Controller,” on page 105 specifies the requirements for the PS/2 style keyboard and mouse interface.
- Chapter 8, “Audio,” on page 113 defines configuration retirements for the audio controller.
- Chapter 9, “ESCC,” on page 115 defines requirements for the enhanced serial communications controller which is the Apple style serial port.
- Chapter 10, “Apple Desktop Bus Controller,” on page 129 defines the requirements for the Apple Desktop Bus™ controller which provides the Apple style mouse and keyboard interface.
- Section 11, “IDE Drive Controller,” on page 141 sets the requirements for the integrated device electronics controller.
- Chapter 12, “SCSI,” on page 147 describes the small computer system interface requirements.
- Chapter 13, “Graphics,” on page 161 gives the requirements for the graphics subsystem.
- Chapter 14, “Versatile Interface Adapter (VIA),” on page 165 describes the requirements for this legacy Apple device
- Chapter 15, “Descriptor-Based DMA,” on page 171 defines the DBDMA requirements for this Apple legacy controller.
- Appendix A, “VGA Programming Model,” on page 195 is a description of the programming model for the video graphics array which is an IBM PC legacy device.
- Appendix B, “Requirements Summary,” on page 237 is a complete list of all requirements statements imbedded in a chapter level table of contents. This appendix is a useful summary or check list for those implementing CHRP systems.

Suggested Reading

The Bibliography provides a full list of references and ordering information for these references. Within this document, the number of the reference in the bibliography is placed after the citation in brackets, “[nn]”.

This document assumes the reader has an understanding of computer architecture, the PowerPC microprocessor architecture, the current PowerPC processors, Apple and IBM compatible personal computers, Peripheral Component Interconnect (PCI) local bus, and Open Firmware. Some understanding of the current personal computer and workstation architectures is also useful. A list of suggested background reading includes:

- *Computer Architecture: A Quantitative Approach* [3]
- *The PowerPC Architecture: A Specification for a New Family of RISC Processors* [2]. Note that this specification is referred to as *The PowerPC Architecture* in the body of this document.
- *PowerPC 603 RISC Microprocessor User's Manual* [4]
- *PowerPC 603 RISC Microprocessor Technical Summary* [5]
- *PowerPC 604 RISC Microprocessor User's Manual* [6]
- *PowerPC 604 RISC Microprocessor Technical Summary* [7]
- *Technical Introduction to the Macintosh Family* [8]
- *PowerPC Reference Platform Specification,* Version 1.1 [12]
- *PCI Local Bus Specification*, Revision 2.1 [10]
- IEEE 1275, *IEEE Standard for Boot (Initialization Configuration) Firmware, Core Requirements and Practices* [9] and relevant bindings

Conventions Used in this Document

Within the body of this document lists of requirements are clearly defined. The convention used is to head each requirements list with the word "**Requirements:**" in bold face type. Following this heading are one or more requirements. These requirements may point to other standards documents, or figures or tables which conveniently show the requirement. The referenced material becomes part of the requirements in this document. Users of this document must comply with these requirements to build a standard platform. Other material in this document is supportive description of these requirements, architecture notes, or implementation notes. Architecture or implementation notes are flagged with a descriptive phrase—for example, "Hardware Implementation Note"— and followed by indented paragraphs. The descriptive material and notes provide no additional requirements and may be used for their information content.

Big-Endian numbering of bytes is used in this document, unless indicated otherwise.

Numbering of bits starts at zero for the least significant bit and continues to the most significant bit. Diagrams show the most significant bit at the left.

Typographical conventions used in this document are described in Table i on page xxvi.

Table i. Typographical Conventions

Text Element	Description of Use
Italics	Used for emphasis such as the first time a new term is used. Indicates a book title. Indicates PowerPC instruction mnemonics. Indicates Open Firmware properties, methods, and configuration variables. Indicates RTAS function and parameter names
0xnnnn	Prefix to denote hexadecimal numbers.
0bnnnn	Prefix to denote binary numbers.
nnnnn	Numbers without a prefix are decimal numbers.
0xF. . . FFF100	This hexadecimal notation represents a replication of the hexadecimal character to the right of the ellipsis to fill out the field width. For example, the address 0xF . . . FFF100 would be 0xFFFFF100 on a processor with a 32-bit address bus or 0xFFFFFFFFFFFFF100 on a processor with a 64-bit address bus.
0:9	Ranges of bits are specified by two numbers separated by a colon. The range includes the first number, all numbers in between, and the last number.

Table i. Typographical Conventions ***(Continued)***

Text Element	Description of Use
0xm-0xn	A range of addresses or values within the document is always inclusive, from m up to and including n.

Within this document each register is described using a table in the format of Table ii on page xxvii. Within this table the first column gives the size in bytes of the register. The second column gives the type of addressing either “Direct”, “Indirect”, “Sequenced”, or “Mode Selected”. The third column gives the Open Firmware “reg” property which gives the base address of a set of registers. The fourth column, “Offset Address” is the register offset from the base address given by the reg property. The fifth column gives the register read and write characteristics as viewed by the software. The sixth column gives the initial value in the register when Open Firmware passes control to the operating system. The last column gives the value to which the register is reset, if software invokes a reset of that device. For those devices which can not be reset by software, this column is “N/A”

Table ii. Register Characteristics

Register Size	Register Addressing	Associated Reg Property	Offset Address	Read/Write Characteristics	Value in Register when OF passes control to OS	SW Initiated Reset Value
1 byte	Direct	reg[1]	0x00	Read/Write	0x00	0x00

Each chapter has a table similar to Table iii on page xxvii which indicates that a particular device is required or optional in a configuration for different platform types. The table does not indicate that the architecture is optional. If a device is present, then the architecture must be as described in this CHRP I/O document. This short table in each chapter is excerpted from Table 2 on page 19 in the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* [1]. An explanation of this table and the symbols used in it is given in Section 2.5.1, “Table Description,” on page 17 in the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* [1] document. For convenience, the legend used in the table is repeated below:

- R: Required.
- R*: Entries categorized as R* denote specifications from which platform vendors may *choose* one or more to satisfy the requirement. All R* specifications are supported by portable and personal CHRP operating systems.
- O: Optional (refer to the definition of optional given in Section 2.6, “Options and Extensions,” on page 20).
- M: Required for systems designed to run Apple Mac OS.

Table iii. Minimum Requirements for Alphanumeric Input Device and Pointing Device

Subsystem	Specification	Portable	Personal	Server	Description
Alphanumeric Input Device		R	R	O	Servers do not require a keyboard for normal operation, however a means to attach an A/N Input Device must be provided; an ASCII terminal is a example of such a device. Keyboards must be capable of generating at least 101 scan codes.
	PS/2 Keyboard interface	R*	R*	O	
	ADB	R*	R*	O	
	Terminal	O	O	O	

Table iii. Minimum Requirements for Alphanumeric Input Device and Pointing Device ***(Continued)***

Subsystem	Specification	Portable	Personal	Server	Description
Pointing Device		R	R	O	If a platform includes a keyboard, it must also include a pointing device with the functionality of at least a 2-button mouse
	2 buttons	R	R	O	
	PS/2 interface (see note 1)	R*	R*	O	
	ADB	R*	R*	O	

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Comments on this Document

Comments on this document are welcome. Because of time and resource constraints, we will not always be able to provide responses to general industry comments. We will review your comments for possible incorporation in future versions of the specification. All comments become the property of Apple, IBM, and Motorola and may be used for any purpose whatsoever. For this reason, comments must not contain any proprietary data. Please preface your comments with the statement "These comments do not contain confidential or proprietary information and may be used for any purpose". Comments may be addressed to:

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